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An Improved Methodology for Sample-Time Calibration in Time-Interleaved Analog-to-Digital Data Converters

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Abstract

A mixed-signal scheme is presented for the sample-time error calibration in time-interleaved analog-to-digital converters (TIADC). Interchannel equalization is used to remove the sample-time error mismatch between channels using an extra channel. Simulation results show that the proposed technique is able to improve the SNDR for a 12-bit TIADC system by 29 dB at 37% of the Nyquist rate frequency.

***Keywords*:** Pipeline A/D converter, Time-Interleaved ADC, Mixed-Signal Calibration

1. Introduction

Time-interleaving increases the effective data conversion rate in analog-to-digital converters while keeping the circuit requirements the same for a desired speed. However using this technique needs special considerations as other design issues associated with using parallel identical channels emerge. The first and the most important is the problem of timing mismatch between channels. This error is also called sample-time error, which can directly affect the performance of the ADC. Many techniques have been developed to tackle this issue both in analog and digital domains [1]-[3]. Most of these techniques have high complexities especially when the number of channels exceeds 2 and some of them are only valid when input signal is a single tone sinusoidal. This would limit the application for which these techniques can be used. The proposed technique in this brief bests the previous techniques in terms of simplicity. It can also be used with arbitrary input signals. This is a merit of the design and broadens its application.

Sample-time calibration of TIADCs consists of error detection and correction. Error correction is more straightforward and can be done in analog, using a Variable Delay Line (VDL), or in the digital domain, using an adaptive FIR filter. The detection part is more difficult and is best done in digital domain. The proposed technique focuses on the detection part of sample-time error minimization.

2. Proposed Calibration Scheme

In time-interleaved ADCs different channel mismatches which degrade the performance are offset, gain, and sample-time error. If sampling-time error is approximated by $\Delta V_1 = \frac{dV_{i,1}}{dt} t_1$, then

$$V'_{o,1} \approx G_1 V_{i,1} + \frac{dV_{i,1}}{dt} t_1 + V_{off,1}. \qquad (1)$$

In (1), is the gain error, is the sample-time error, and is the offset of the first channel. The proposed technique uses an extra channel to detect the sample-time error between the extra channel and each channel of the ADC and hence removes the mismatch between among all the channels. Fig. 1 explains how the proposed technique is working. It should be mentioned that the extra channel does not need to be error free channel and it could be a normal copy of the regular channels of the ADC. Also, the clocks do not need to be aligned precisely since it is already included in the sample-time error and the calibration procedure will remove this error.

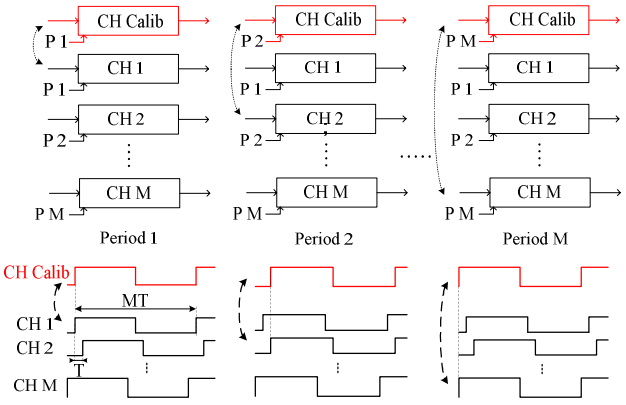


Fig. 1: The proposed technique uses an extra channel to detect the sample-time error of each individual channel in each clock period.

The extra channel here is referred to calibration channel, CH_{Calib}. Each ADC channel which needs to be calibrated is called, $CH_{ADC,j}$ (j=1, 2, …, M). In each clock period, the calibration channel mimics the operation of the ADC channel which is under calibration. This means the two channels are using the same input signal and the same clock phase. If only sample-time error is present at the output, the difference between the outputs of these two ADCs can be written as:

$$V_{o,2} - V_{o,1} = \frac{dV_i}{dt}(t_2 - t_1). \qquad (2)$$

Thus, the subtraction of the two outputs is directly proportional to the sample-time mismatch between the two channels. Since mismatch also depends on the input signal, it cannot be used directly. In order to remove the effect of the input signal we take discrete integral of (2). The result includes a constant value, K, and a term which is proportional to the sample-time mismatch between the two channels

$$\sum_n \Delta V_{O,21} = \Delta t_{12} K + \Delta t_{12} \sum_n \frac{dv_i}{dt}. \qquad (3)$$

In order to use this expression as input to the correction circuit, we need to reduce the effect of the rightmost term in (3), which is varying with the input. This could be done by multiplying (2), by a very small value before taking the integration. This procedure is shown in Fig. 2. The term which includes the input signal does not have any effect on the value to be used for the correction. Therefore, this technique could be used with arbitrary input signal. After integration, the result is used as the input to the correction circuit which is implemented digitally using a look-up table (LUT) and an FIR filter. The FIR shifts the output of one calibration channel in the time domain [4]. After specific amount of clock cycles, the output of the accumulator converges to the value which is proportional to the sample-time mismatch between the two channels and hence the mismatch between the two channels is removed using the adaptive FIR filter.

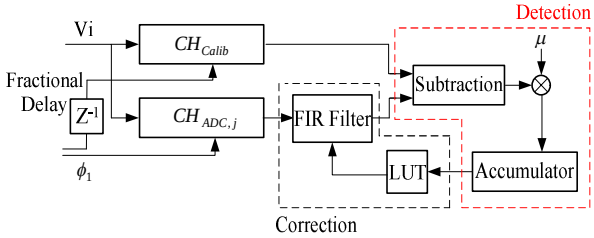
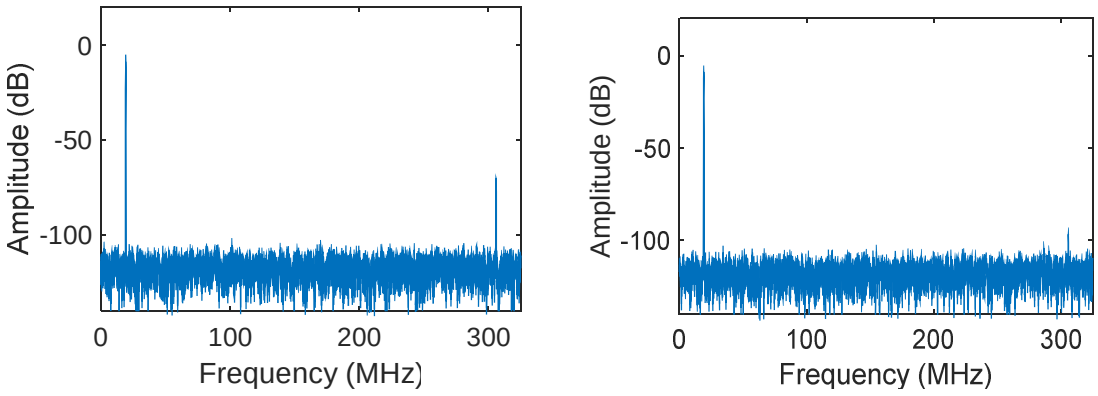


Fig. 2: The proposed sample-time calibration technique.

The proposed technique does not use any correlation function or Hilbert transform for sample-time error detection. This considerably simplifies the calibration procedure compared to some prior techniques [2] and [5]. Also, unlike some other techniques such as [3], this technique could be generalized to an arbitrary number of channels without adding extra complexity.



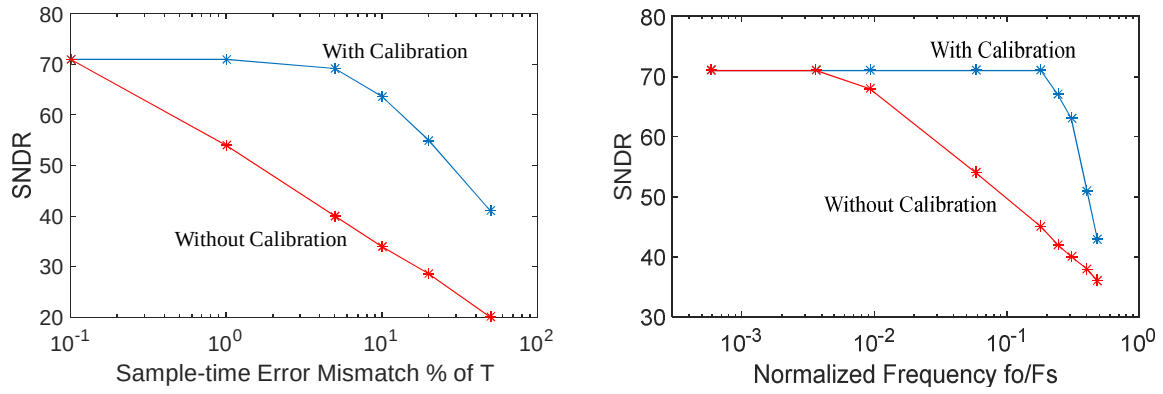
a) b)

Fig. 3 The simulated output of the overall ADC using the proposed technique. a) Before calibration, b) After calibration.

For an M-channel TIADC, the mismatch between each channel and the calibration channel can be shown as $\Delta t_1, \Delta t_2, \ldots, \Delta t_M$. Since all channels are calibrated with one channel, using the same procedure as explained above, the mismatch between the channels will also be removed. As mentioned before, this technique is able to correct errors for arbitrary input signals, while some other techniques could only be used with single-tone input signals. Also assumed is that offset and gain error are first calibrated using one of many prior proposed techniques [4].

3. Simulation Results

To demonstrate the validity of the proposed technique, a two-channel 12-bit 325-MS/s ADC is designed, implementing the calibration techniqueThe calibration engine consists of calibration channel, detection and a correction circuitry for each ADC channel. For the correction part, a similar approach as in [4] is used. An LUT which generates the coefficients of the FIR filter according to the input and an FIR filter which shifts the output of the channel in the time domain with a fractional delay. A 20-tap FIR filter is used here. Fig 3 shows the simulation results. Fig 3a and b show the output spectrum before and after calibration for $\Delta t/T = 0.01$. As these figures show, the unwanted image due to sample-time error has been considerably suppressed from the output using the proposed technique. The SNDR has been improved from 59 dB to 70.8 dB. Fig 4a shows the SNDR vs. sample-time mismatch as percentage of the ADC sampling period $\Delta t/T\%$, with and without the proposed calibration technique.



a) b)

Fig. 4: Performance of the proposed technique. a) SNDR vs the sample-time error mismatch, with and without calibration. b) SNDR vs Input Frequency with and without calibration.

As this figure shows, the proposed technique is able to improve the overall performance for the error mismatches up to 20% of the sampling period by 26 dB and achieve around 21 dB improvement for a mismatch of 50% of the sampling period. Since the input is a narrowband sinusoidal signal a large mismatch error is considered. For wideband signals the matching constrains are more relaxed [6]. Fig 4b shows the improvement of SNDR using the proposed technique for different input frequencies close to $F_s/2$. As this figure shows, the improvement is up to 26 dB at 37% of the Nyquist frequency. It should be mentioned that in order to save the overall power consumption of the ADC, the calibration channel could be turned off after the calibration procedure has been done.

4. Conclusion

A sample-time error calibration technique has been proposed which uses an extra channel to detect the sample-time mismatch between the channels. The proposed technique decreases the complexity of the calibration ystem and could be used with arbitrary input signals. A design example of a 12-Bit TIADC shows that the proposed technique is able to improve the SNDR by 20 dB for a mismatch of 50% of the sampling period and up to 29dB at 37% of the Nyquist frequency.

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